APPLICATION CONFIGURABLE SYSTEM CELLS

Description

Application Configurable System Cells (ACSCs), have been developed by Dialog Semiconductor for specific market segments. The System Cells consist of primary groups of function blocks which have been targeted at individual applications. The Design Engineer is able to utilize these blocks to build his system, and if necessary, have them customized by Dialog to exactly meet his requirements. Proven ASIC design and process technology mean that the circuits provide cost-effective and extremely reliable solutions to manufacturers within a variety of fields. Manufacturers benefit from a highly developed application-oriented product, with the added advantage that while it can be fully customized, both development times and risk factors can be significantly reduced. The concept allows the Design Engineer to build a system from proven high level circuit blocks, rather than designing at the standard cell or transistor level.

In any given market place the main participants are usually offering similar products. They differentiate themselves by offering variations on price, performance or functionality. One of the ways they can achieve differentiation is by developing ASICs which encapsulate these benefits. However, many of these would-be users of ASICs may be put off by what they perceive as risk or expense or long development time. In other words the end result, in Dialog's case a mixed signal ASIC, may be very desirable but getting there may seem daunting, even though mixed signal developments are, these days, rarely problematical.

So what is required by many system companies is a kind of 'instant ASIC' - the end result without the pain. With this in mind, Dialog has developed its ACSC strategy. ACSC is an attempt to distil the key attributes of a given application into high level cells to which systems developers have access. By analyzing the common features of a market or application and then pre-developing the main blocks most of the risk and much of the time element is removed from the equation. Individual systems developers can add as much or as little to the ACSC blocks as they wish. Indeed, the ACSC blocks can be used in standalone mode as discrete ICs, if preferred and, in fact, this may be the best way to start.

A system developer can design-in an ACSC like an ASSP and even go into production with it. As more is learned about the system, or if market feedback suggests it, changes may be required. With any sort of ASSP or standard product, changes are a major problem and can be lengthy and expensive. The ACSC, however, is designed to be flexible and modifying its performance or behaviour is intended to be straightforward. At heart, the ACSC is a technology demonstrator and adding circuitry around it is welcomed as a way of introducing more companies to the benefits of mixed signal ASICs

As part of its programme, Dialog Semiconductor can provide User Evaluation Boards, so that the designer can part-develop his system, using the proven System Cells in conjunction with other system components. ACSCs developed by Dialog Semiconductor are targeted to vertical markets, for example, Satellite Communications, Video, Automotive, Security, and Utilities Metering applications.

Dialog has had extensive ASIC experience in the communications field. Using this experience, Dialog has created a range of Major and Minor ACSC blocks to support our customers in specifying and designing ASICs for their communications products.

In summary ACSCs are:

- A group of 'Expert Cells' targeted to a specific application
- A fully characterized mixed signal sub-system
- Usually available as packaged parts

Main benefits for the system user:

- Allows complete system development when used with field programmable parts
- Short development time
- Can be used to assess market
- Can be used for initial production
- Reduced Technical Risk

DTMF GENERATOR

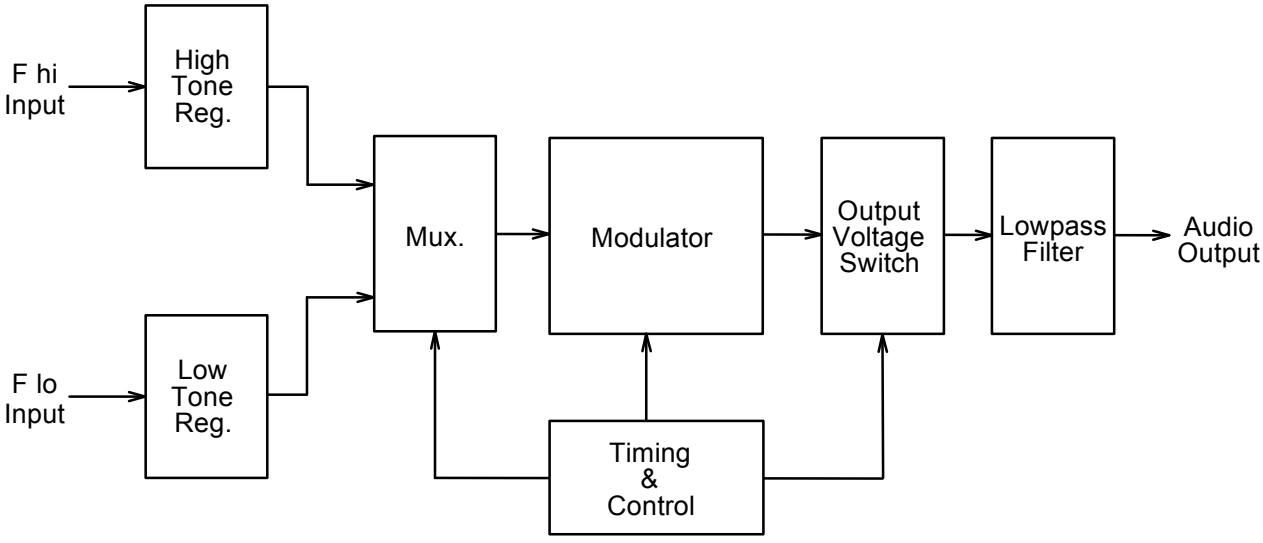
Description

This major ACSC function employs an oversampling frequency synthesiser in an interleaved mode to produce dual-tone multi-frequency (DTMF) telephone dialling tones. The synthesiser is based on direct digital synthesis using phase accumulation with the high and low tone frequency divisors held in separate input registers. The digital to analog conversion is carried out using a first order sigma-delta converter which interleaves the high and low tone samples. The 1-bit datastream switches two bi-polar voltage levels to produce the fixed tone twist for the CCITT specification. The output is then filtered using a simple 2nd order lowpass filter to regenerate the audio signal.

Features

- Low power requirements - logic based
- Small size
- Perfected for mobile communications applications

Functional Block Diagram



SERIAL INTERFACE ADAPTOR (LANCE)

Description

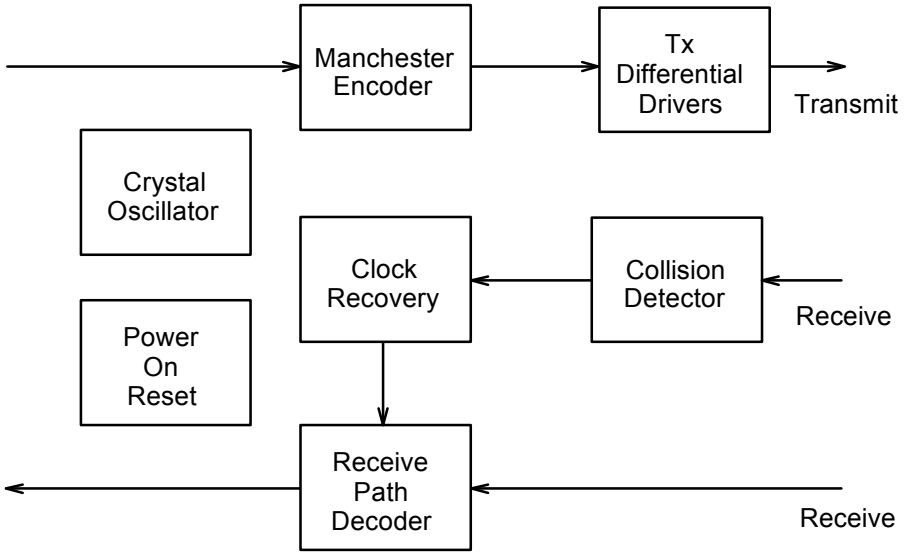
This major ACSC function is an IEEE 802.3/Ethernet compatible Manchester Encoder / Decoder, that integrates all functions to interface Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable. It has two sections, transmitter and receiver. The transmitter uses Manchester encoding to clock data into a serial bit stream, differentially driving up to 50m of twisted pair transmission line. The receiver detects the presence of data and collisions. The receive clock is recovered from the incoming bit stream by a phase locked loop and is used to decode the Manchester bit stream into data.

The cell can be programmed to operate in one of two variants compatible with the SIA types 8023 and 7992.

Features

- Compatible with Ethernet/IEEE-802.3 specifications
- 20 MHz parallel resonant crystal oscillator
- Manchester Code Encoder and Decoder
- Phase Locked Loop Clock Recovery
- Loopback Diagnostic Test Capability
- Receiver and Collision Squelch Circuit guarantees operation at inputs >±275mV and with no operation <±160mV
- Emulates most common SIA alternatives

Functional Block Diagram



CODEC

Description

This major ACSC function implements a 13 bit 8kHz PCM speech encoder/decoder and the associated speech channel filtering using a sigma delta modulator and DSP techniques.

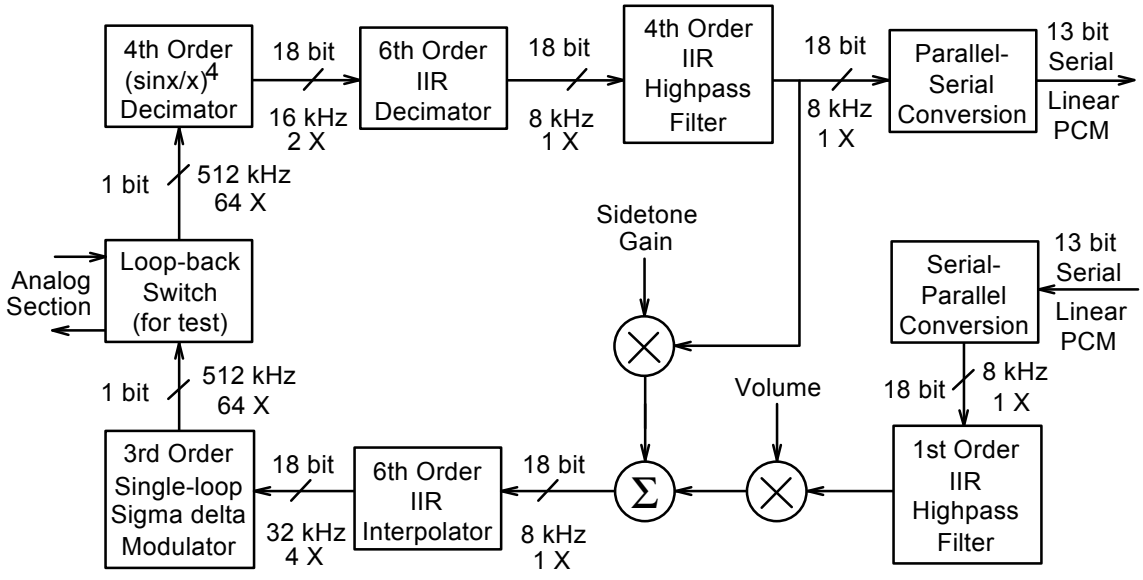
The sigma delta modulator oversamples at 512kHz, which is decimated to 16ksps in a $(\sin x/x)^4$ filter. The encoding channel filter is a 10th order band pass filter.

The input data is scaled by the volume control and the sidetone (also programmable level) is added. The decoding channel filter is a 6th order lowpass at 32ksps which is followed by a digital sigma delta modulator to generate the 512kHz bit stream which is converted to analog, filtered and output.

Features

- 13 bit 8kHz PCM speech codec and filters
- Sigma delta modulator / DSP implementation
- Meets CCITT filter requirements
- Programmable receive volume
- Programmable Sidetone
- Scalable to lower operating voltages
- Used in telephone / mobile handsets

Functional Block Diagram



SPEECH COMPANDER

Description

This major ACSC function processes telephone bandwidth (300Hz to 3.4kHz) audio signals according to a 2:1dB logarithmic law. The compression and expansion processes use the same basic cells in a different configuration.

The compressor uses a delta-sigma converter with variable reference voltage generated by full wave rectifying and filtering the audio output. The bit stream data is then multiplied by a fixed reference voltage and the audio output generated by the reconstruction filter.

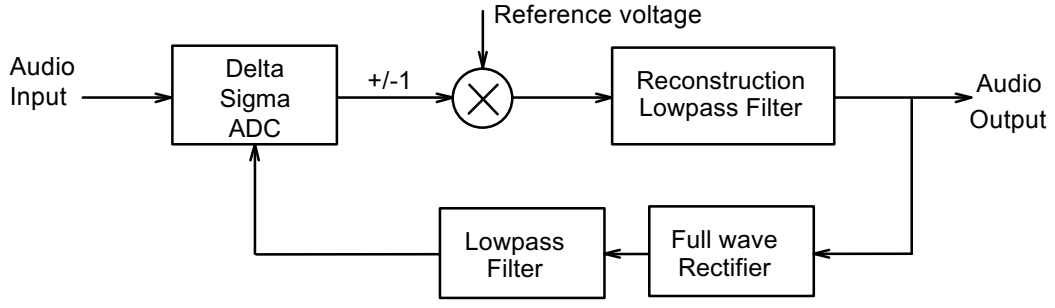
The expander uses a delta-sigma converter with a fixed reference voltage. The input is also full wave rectified and lowpass filtered to give a variable reference. The bit stream data is then multiplied by the variable reference and the audio output generated by the reconstruction filter.

Features

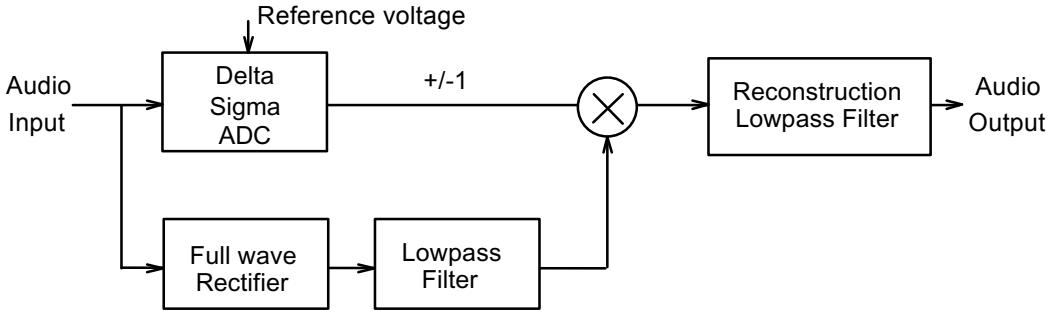
- Small size
- Implemented on CMOS technology
- Low external component count

Functional Block Diagram

COMPRESSOR



EXPANDER



OVER-VOICE MODEM

Description

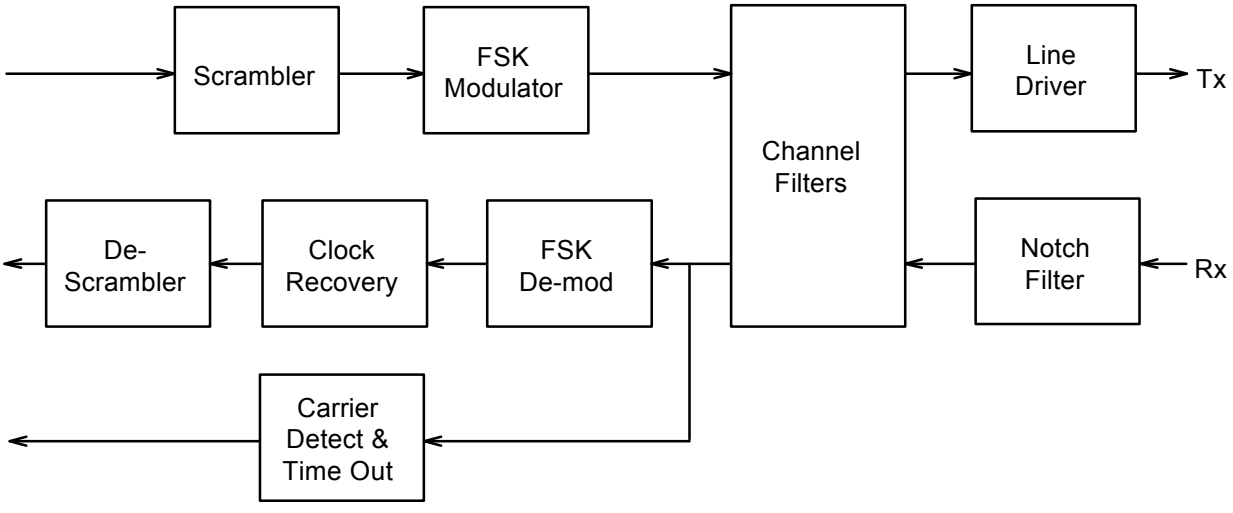
This major ACSC provides all the functions required for an 'over-voice' modem, which transmits and receives data at 4800 baud over the standard telephone line such that the data channel does not interfere with normal voice communication. The transmit portion of the circuit employs phase coherent FSK modulation using a synthesised sine wave to produce a Space tone at 17.55KHz and a Mark tone at 21.94KHz. The modulated signal is band-pass filtered and buffered before application to the line. Operation is in half-duplex mode and synchronous or asynchronous transmission can be selected. In synchronous mode the data is scrambled.

The receive function includes switched capacitor filters for filtering the FSK signal and rejecting the 12KHz Pay-tone, a zero-crossing detector and digital demodulator, the demodulated signal is reconstructed via a switched capacitor low-pass filter and a comparator. There is also a carrier detect circuit which detects that the carrier is of correct frequency and amplitude for operation of the receiver.

Features

- Phase coherent FSK modulation
- Transmission rate 4800 baud
- Half-duplex synchronous / asynchronous operation
- Carrier detection
- No external filter components
- +5V single supply
- Low consumption 4mA typical
- Loop-back mode for testing overall functionality

Functional Block Diagram



SPEECH SCRAMBLER/DESCRAMBLER

Description

This major ACSC function performs scrambling and descrambling operations on speech (300Hz to 3.4KHz) signals. The input speech signal is filtered into four bands which are then modulated onto one of the other bands with or without frequency inversion, thus resulting in approximately 100 usable scrambling codes. The de-scrambler is used to restore the original speech after transmission.

The input is first filtered by on-chip CT anti-alias filters prior to anti-alias filtering by a switched capacitor filter for the sampling rate used in the signal path also by use of switched capacitor circuitry. The input filter bank consists of four filters which split the speech into four bands of 800Hz.

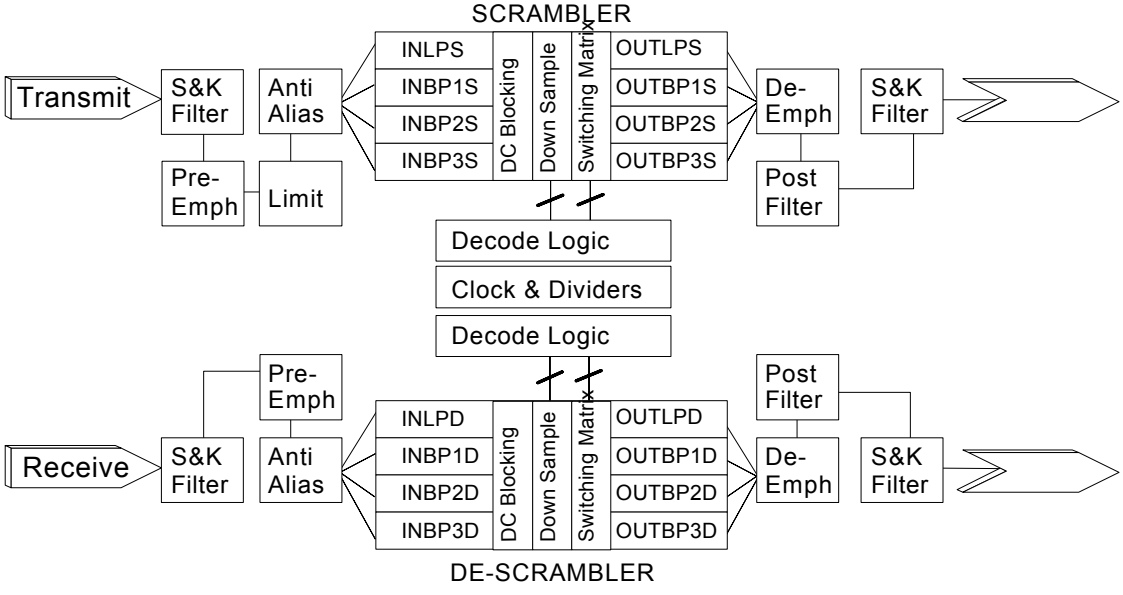
To avoid tones at the carrier frequencies caused by DC modulation, DC offset cancellation is included in each path. A matrix of switches is provided to enable any input channel to be routed to any output channel and is controlled by an 8-bit word. Each input frequency band is down-sampled by taking every eighth sample and discounting the intervening samples. By multiplying alternate samples by -1 a frequency shift of 800Hz is obtained and it possible to map an input band onto any output band. Output filters are adjusted to give the required sin(x)/x correction due to the sampling rate.

The four output bands are summed prior to the de-emphasis filter and, on the transmit side, this results in a scrambled speech signal - on the receive side de-scrambled speech is obtained.

Features

- Functions from single 5V supply
- Less than 6mA power consumption
- Contains both scrambler and de-scrambler on one chip
- Contains all filters on this single chip
- Very few external components
- Controlled via serial interface
- For commercial specification security systems
- For use in both base-stations and mobile handsets

Functional Block Diagram



SWITCHED CAPACITOR FILTERS

Description

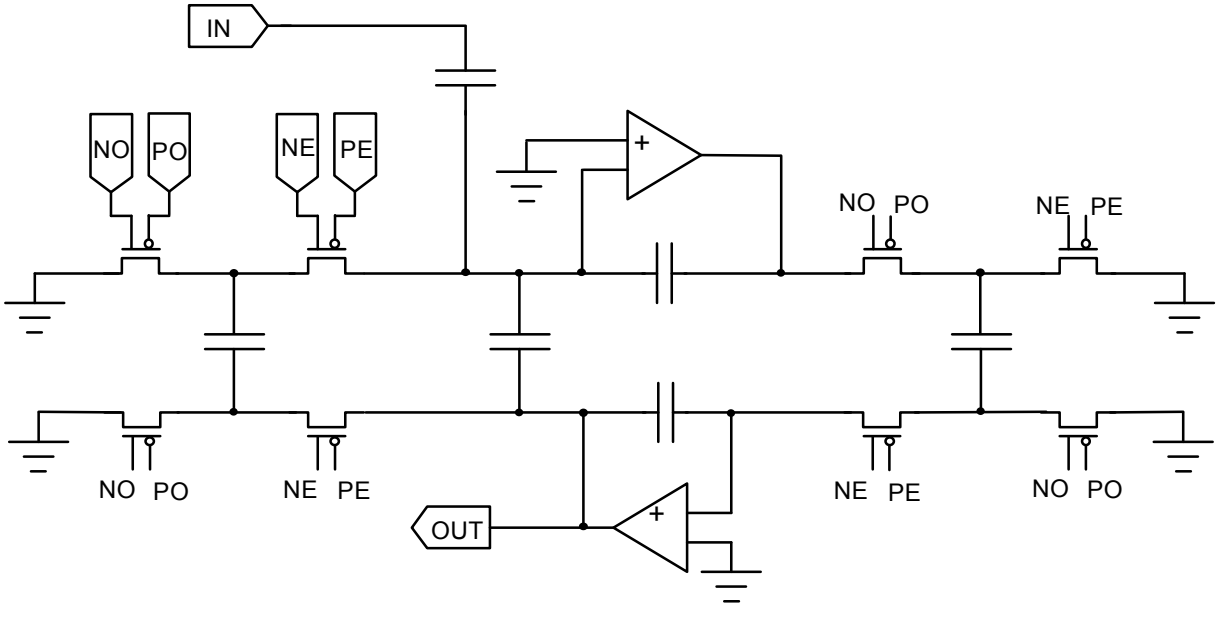
By using state-of-the-art CAD tools for design, synthesis and simulation of sample-data filters either cascaded biquad or RLC ladder filters may be provided using switched-capacitor realisations with orders from 1 to > 12. For flexible, programmable and area-efficient filter structures, any number of 1st, 2nd and 3rd-order biquad sections may be cascaded and then simulated for effects of supply voltage, process and temperature variations prior to synthesis.

Dynamic range and frequency response can be extended by use of fully differential structures. Sin(x)/x, warping and aliasing effects are reduced by pre-warping the filter response and by use of 2nd or 3rd order continuous-time (active RC) filters which are included on chip. Filter sensitivity is reduced by use of ladder, rather than cascaded biquad, SCF structures. Non-overlapping clock phases required by the SC switches are generated using standard cell circuits.

Features

- Handles signal frequencies from <0.1Hz to >250kHz
- Uses on-chip anti-aliasing filters
- No external (off-chip) components required
- Either ±5v, +5v or +3v supplies may be catered for
- Clock phases generated on-chip from just one external (stable) clock
- Gains and pole positions accurate to within 0.05%
- Filters, integrators, differentiators, rectifiers and companders may be realised

Functional Block Diagram (2nd Order Biquad)



DIGITAL FILTERS

Description

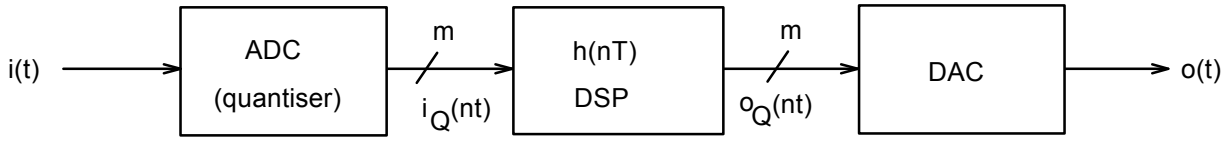
When reproducible, accurate and/or programmable filtering is required in a single-chip solution a digital filter should be considered. Using state-of-the-art design tools and technologies, DSP solutions can be provided to a wide range of datacom, telecom, audio, medical and consumer requirements. These may be used in conjunction with mixed-signal cells such as amplifiers, CT-filters, ADCs and DACs as exemplified in the schematic below. Using Mentor Graphics' DSP Station the filter is designed, optimised and simulated at gate/block level for a bit-true realisation.

Finite word-length analysis, limit-cycle investigations and noise analyses are carried out prior to transfer for ASIC routing tools for area-efficient synthesis. VHDL may also be used for design entry, simulation or logic synthesis. Code is generated for use in prototyping (FPGA or DSP board) when hardware is required prior to silicon availability.

Features

- Filters of virtually any order may be realised
- Supply voltages of 2.7-5v catered for
- Supported by prototyping
- Operation may be programmable
- FIR or IIR
- Adaptive filters
- May be used in conjunction with on-chip data-converters for analog-in/analog-out integration

Functional Block Diagram



OSCILLATOR FOR CERAMIC RESONATORS

Description

This minor ACSC is a 2-pin oscillator based on a single-stage class A amplifier. This minimises the output voltage swing and therefore current/power dissipation.

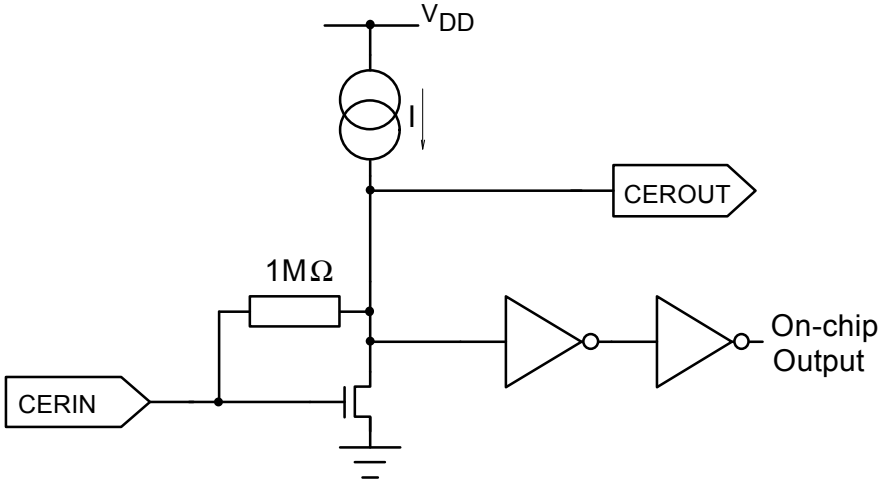
An internal 1MΩ (nom.) feedback resistor is provided, saving an external component. The oscillator cell, when used with a resonator with integral load capacitors provides a low-cost and compact stable timebase for many applications.

At 4MHz, I_{DD} < 200µA (nom.)

Features

- 2 pin oscillator, well suited for use with ceramic resonators
- Frequency range 0.5MHz to 4MHz
- Feedback resistor (1MΩ) on-chip saves external component
- Operating current 200µA or less

Functional Block Diagram



CRYSTAL OSCILLATOR

Description

This minor ACSC function is a 2-pin oscillator intended for use with crystals and ceramic resonators.

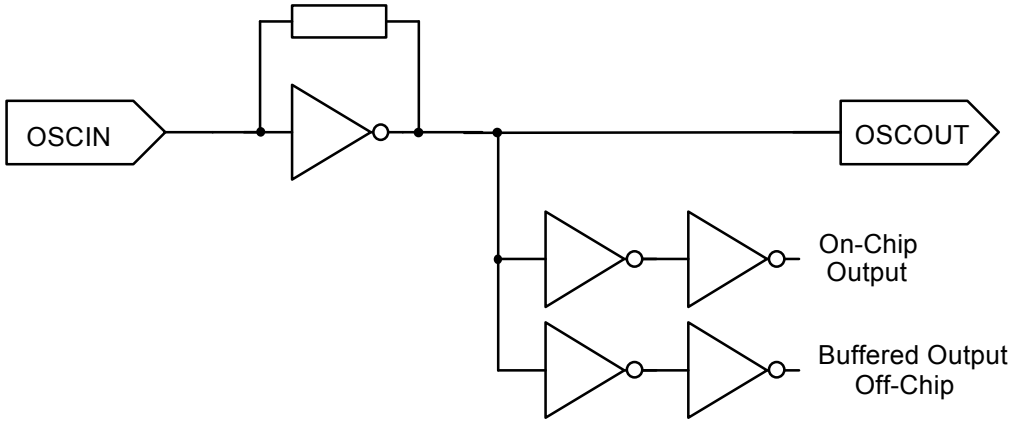
An internal 1 MΩ (nom.) feedback resistor saves an external component and simplifies board layout.

The output of the oscillator can be buffered and brought off-chip through a suitably-sized driver to provide a system clock to the rest of the board.

Features

- 2 pin oscillator, suited to use with ceramic resonators from 6 to 12MHz, or crystals up to 20MHz
- Internal 1MΩ (nom.) feedback resistor saves external component
- Operating current with 12MHz resonator typically 1.5mA

Functional Block Diagram



RC OSCILLATOR

Description

This minor ACSC function is a 1-pin relaxation oscillator. Frequency variations for f < 1KHz is primarily set by external components.

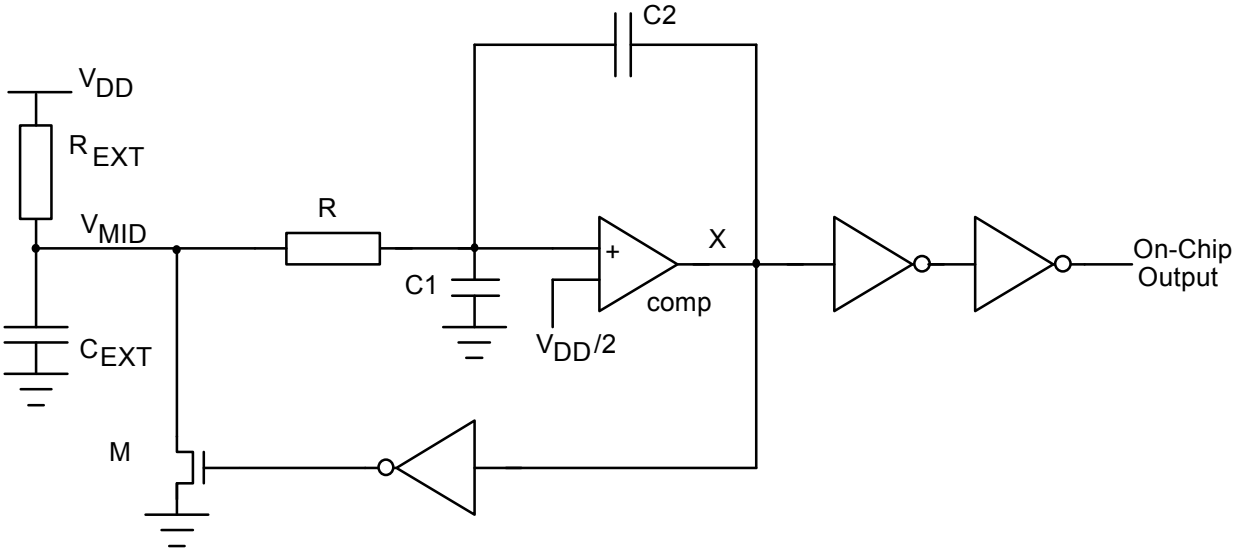
$$t_{osc} = 0.693\ (R_{EXT}\, C_{EXT} + 6\mu s)$$

As V_{MID} crosses VDD/2, comp output x goes high, switching on the pull down device M, for time RC1, completely discharges V_{MID} to 0V. M then switches off, causing V_{MID} to charge up towards VDD again.

Features

- Single-pin oscillator, suitable for generating low-frequency clocks (<1KHz)
- Frequency determined by external R and C
- Low operating current for R = 1MΩ, C = 4.7nF, f = 310Hz, I_{DD} = 35µA

Functional Block Diagram



LOW IMPEDANCE AUDIO DRIVER

Description

This minor ACSC function is an audio frequency 3 stage buffer with ± 12mA output current capability designed specifically to drive low impedance loads such as dynamic transducers.

A double folded cascode input stage provides high front end gain for the intermediate common mode gain stage.

Complementary source followers provide gate drive to the output MOSFETs whilst minimising crossover distortion normally associated with class B output stages.

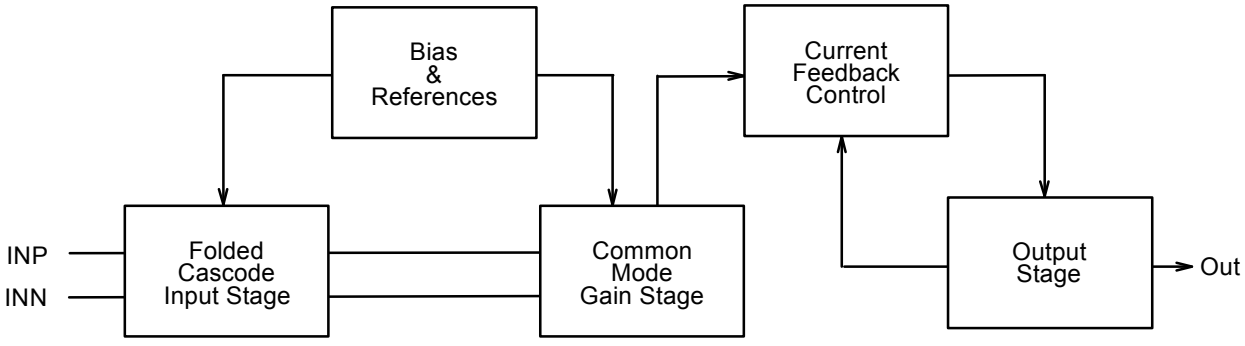
Supply current is minimised by use of a quiescent current feedback control block which monitors the output device current and adjusts the drive to the source followers whilst maintaining stability.

The buffer is internally compensated and will drive capacitive loads up to 100pF rail to rail.

Features

- High current drive buffer provides 4Vpp output into 180Ω with <0.5% THD (Vdd ≥ 4.8V)
- Three stage design with current feedback control only takes 300µA typical quiescent current
- 105dB open loop gain 200KHz unity gain bandwidth 90dB PSRR at 1KHz
- Pair of drivers may be used to drive load differentially

Functional Block Diagram



LOW NOISE AUDIO AMPLIFIER

Description

This minor ACSC function is a MOSFET input low noise amplifier with rail to rail output buffer, designed for audio applications requiring a high input impedance.

The front end consists of P-channel cascoded input devices which have been sized with their loads to provide low flicker noise (1/f knee <100Hz).

Noise performance is suitable for telephone applications; equivalent input referred noise from 50Hz - 3.4kHz is 1.6µVrms. Supply rejection exceeds 80dB across this band.

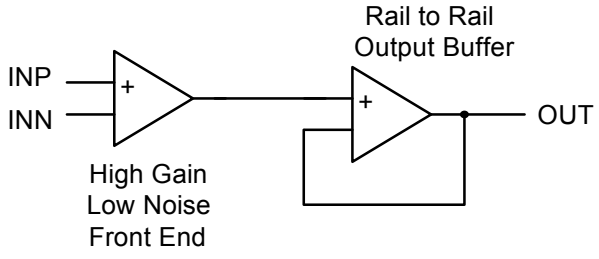
Thermal noise is <25nV/$Hz^{1/2}$.

The output buffer provides low distortion (<0.05% THD) for +/- 2.0V in to 10kΩ/50pF.

Features

- High input impedance, low noise audio amplifier
- Configured with gain for optimum low noise audio path
- Cascoded front end provides >80dB PSRR up to 4kHz
- Equivalent flat input referred noise typically 27nV/$Hz^{1/2}$ over telephone bandwidth
- Supply current = 320µA, Vdd(min) =4.8V
- Open loop gain = 120dB, Unity Gain BW = 1MHz

Functional Block Diagram



RAIL TO RAIL AMPLIFIER

Description

This minor ACSC function is an internally compensated, unity gain stable buffer.

True rail to rail operation is achieved by twin input stages with a low-gm, low distortion input crossover stage.

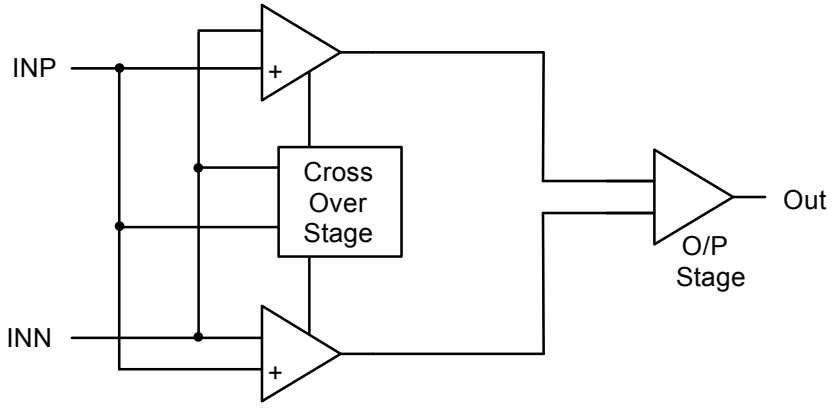
The pseudo push-pull output stage provides low distortion with low (250µA) quiescent current.

Open loop gain and bandwidth are 96 dB, 1MHz respectively.

Features

- Dual input stage gives rail to rail input common mode range
- Rail to rail output for capacitive loads up to 50pF
- $\pm$1.9V into 10KΩ load; $\pm$ 0.7V into 2.5KΩ load (Vdd=4.8V, THD$\leq$30m%)
- Low supply voltage (2.7V) capability with rail to rail operation
- Higher output drive variant available ($\pm$2.1V_{pk} into 1KΩ, Vdd=4.8V, 500µA quiescent)

Functional Block Diagram



MID-REFERENCE BUFFER

Description

This minor ACSC function is a unity gain analog ground buffer with complimentary source follower outputs, providing matched output current capability.

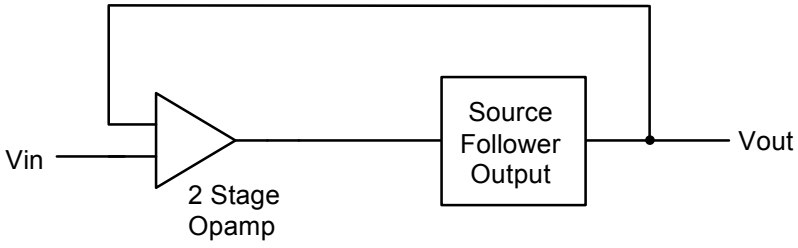
Internally compensated to remain stable for capacitive loads up to 100pF.

Nominal open loop gain and bandwidth is >75 dB and 600KHz respectively.

Features

- Less than 0.1% load regulation at 2.5V for 2.4mA output current
- Equal output current source and sink capability
- Low quiescent current 250µA
- High input resistance from MOSFET inputs

Functional Block Diagram



8 BIT GENERAL PURPOSE DAC

Description

This minor ACSC function is a medium speed CMOS 8 bit resistor sub ranging DAC with buffered voltage output.

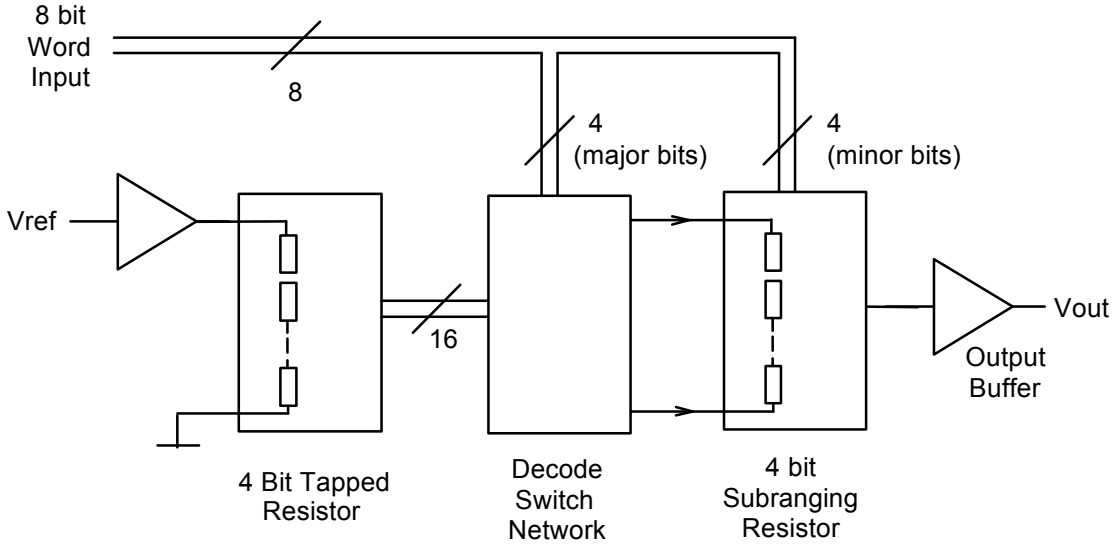
Depending on the input code a 16 element sub ranging resistor (SubR) is connected across two adjacent taps of a 16 element tapped resistor. The four major bits determine the position of the SubR resistor on the tapped resistor whilst the minor bits decode the sub ranging resistor itself.

The tapped resistor is connected between an internal reference and ground in order to ease the input common mode range requirements of the output buffer.
The choice of the output buffer is dependant on the load and speed requirements: e.g. 2µs settling into 200pF with 5V output range.

Features

- CORE settling time = 1µs typical
- ± 1/2 lsb differential non-linearity
- Full scale output adjustable by varying gain of buffer
- Core quiescent current 400µA typical

Functional Block Diagram



8 BIT GENERAL PURPOSE ADC

Description

This minor ACSC function is a CMOS 8-bit linear successive-approximation charge-redistributed ADC with auto-zero and internal sample and hold.

During the first half of the conversion period, the input signal is buffered and sampled onto a hold capacitor whilst the comparator is auto zeroed.

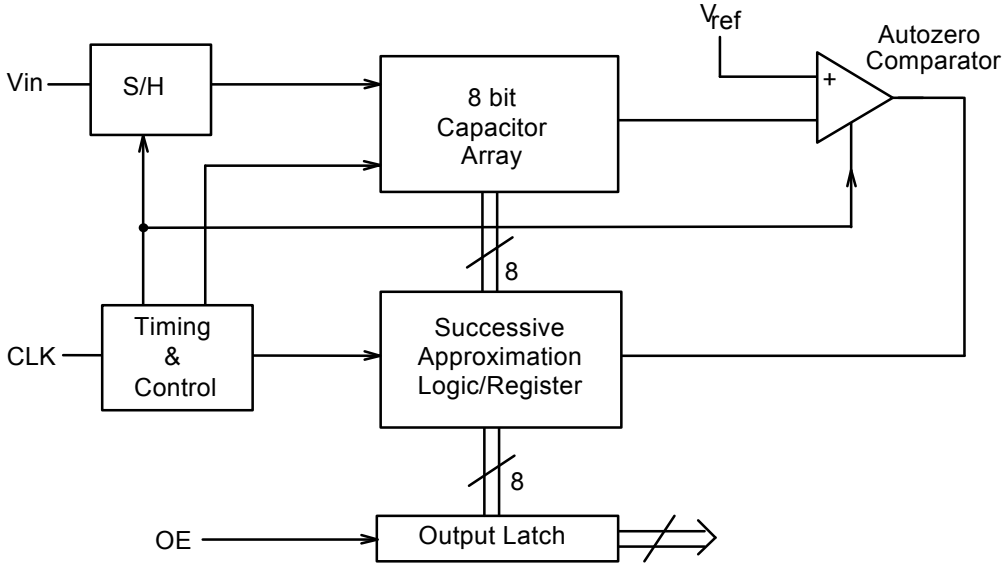
The conversion itself proceeds on a successive approximation basis by sequentially switching progressively smaller capacitors until the output of the capacitor array equals the reference V_{ref}. The switching is controlled by the successive approximation logic which makes a decision for each bit based on the comparator output.

The required 8 bit binary result appears at the output of the SAR block at the end of conversion and may be latched.

Features

- Typical 3µs conversion time
- ± 1/2 lsb differential non-linearity
- 0V to VDD analog input range with sample and hold
- Inputs may be multiplexed
- Slew rate, tracking = 2.5V/µs
- Quiescent supply current 500µA typical

Functional Block Diagram



8 BIT VIDEO ADC

Description

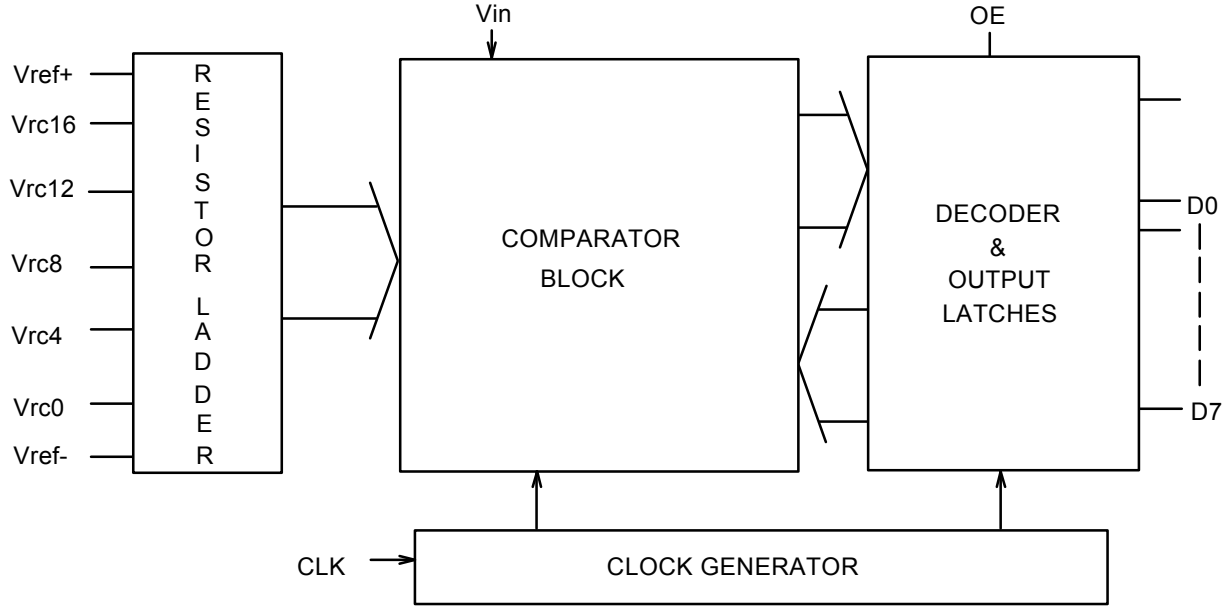
This minor ACSC function is a high speed 8-bit ADC was designed for applications where fast conversions are needed (e.g. for digital video signal processing). To give the best compromise for high speed, low power dissipation and small silicon area, the most suitable structure is a half-flash ADC. The conversion is performed in 3 successive phases. In the first operation, the analog input voltage Vin is sampled. In the second phase, the most significant bits are determined and a DAC converts this coarse digital code to subtract it from the held input. In the last operation, the less significant bits are determined from the remainder of the subtractor and after the complete binary code is latched and buffered in the output latches block. To reduce silicon area, a single multiplexed flash converter performs the coarse and the fine conversions.

This cell was designed in two symmetrical banks corresponding to two 10MHz half-flash ADC operating in a ping-pong arrangement. For some applications only one bank may be enough and therefore the cell is divided by two.

Features

- Operating supply voltage 5V
- Supply current 31mA
- Resolution 8 bits
- Linearity error $\pm$ 0.5LSB
- Conversion rate 200M sample/s
- Full scale range (min) 1V
- Exceptionally small silicon area

Functional Block Diagram



HIGH RESOLUTION ADC

Description

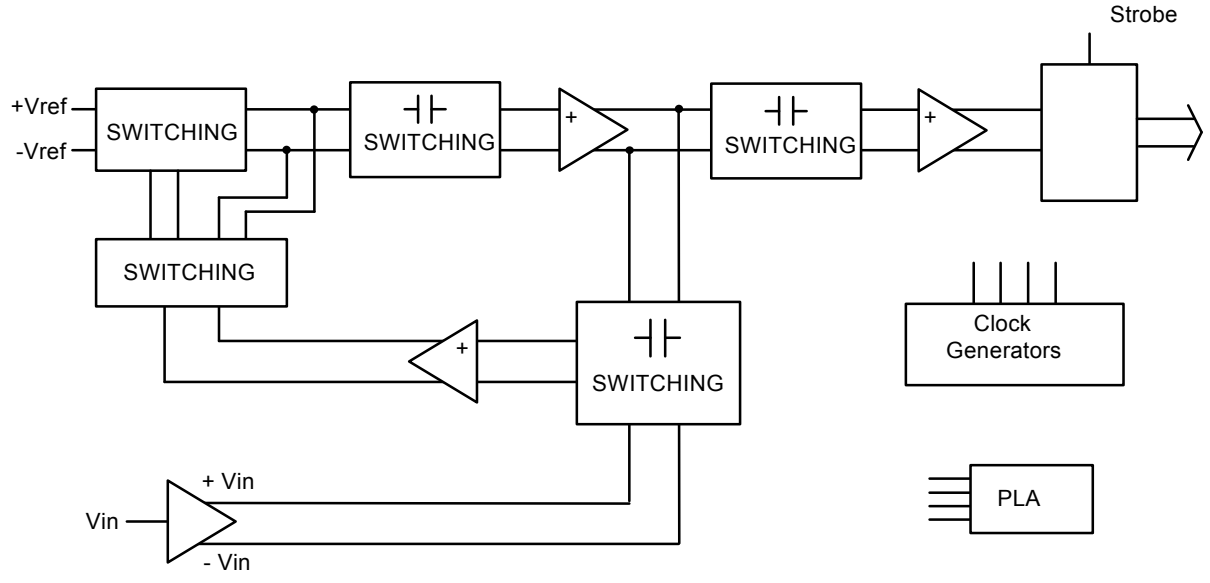
A basic cyclic converter can achieve a limited resolution due to the inaccuracy of the times-2 multiplier, the sample/hold feedthrough, and the amplifier gain used in its construction. This minor ACSC function is a high-resolution converter which removes these inaccuracies while still using the sequential conversion technique of any cyclic converter. Thus the rate of conversion is determined by the required resolution and the settling time but, now, conversion can be made to exceed 12 bits with 1LSB integral non-linearity.

The reference voltage (initially set equal to the MSB) is rotated around the converter loop, interleaved with the normal cyclic conversion algorithm. This causes the reference voltage to be subjected to the same converter loop tolerances (identified above) as the processed signal. This also relaxes the tolerance and size of the capacitors. Each bit of conversion must take 8 clock cycles in this converter and so the 12 bits requires 96 clock cycles in total. The structure used on this chip employs differential circuitry throughout and the capacitors are switched around the opamps to provide the functions of comparison, subtraction and multiply by -2. The switching and sequencing is provided by an on-chip PLA.

Features

- 12 bits resolution
- Single-chip solution with no external components except crystal oscillator
- For datacomms, telecoms and avionic control applications
- Conversion rate of greater than 10KHz
- +/-5V supply
- No "calibrate cycle" required
- Built in sample/hold
- Low power consumption (15mW)

Functional Block Diagram



BAND-GAP REFERENCE

Description

This minor ACSC function is a 1.2µm CMOS Band-gap reference cell for use as an on-chip voltage reference.

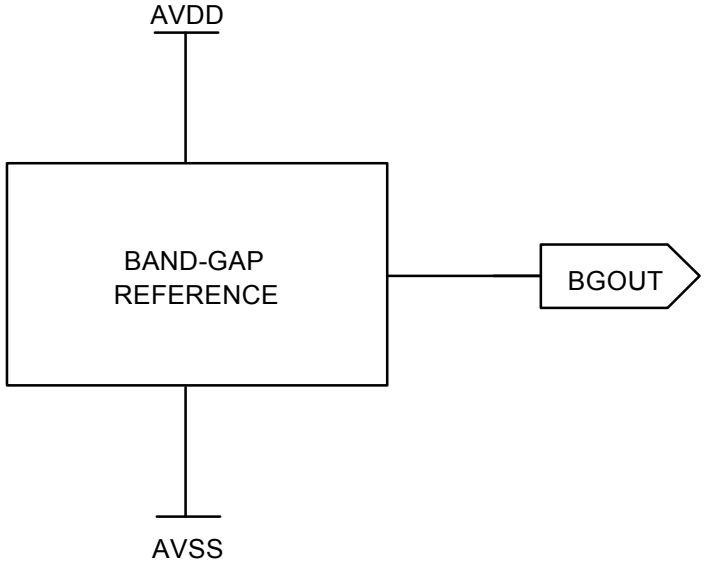
The cell uses vertical pnp transistors in the band-gap cell to reduce output voltage spread. A low offset and low noise bipolar amplifier is used to provide the loop gain.

The cell has an output impedance of 5K ohm so the output should be buffered for load currents exceeding 10µA.

Features

- 1.24 Volt reference +/-4%.
- Supply voltage range 2.5V to 6V
- Temperature coefficient < 100 ppm/^{o}C
- Power supply rejection ratio of >60dB
- Undecoupled output noise < 500µV r.m.s.

Functional Block Diagram



HARD LIMITER

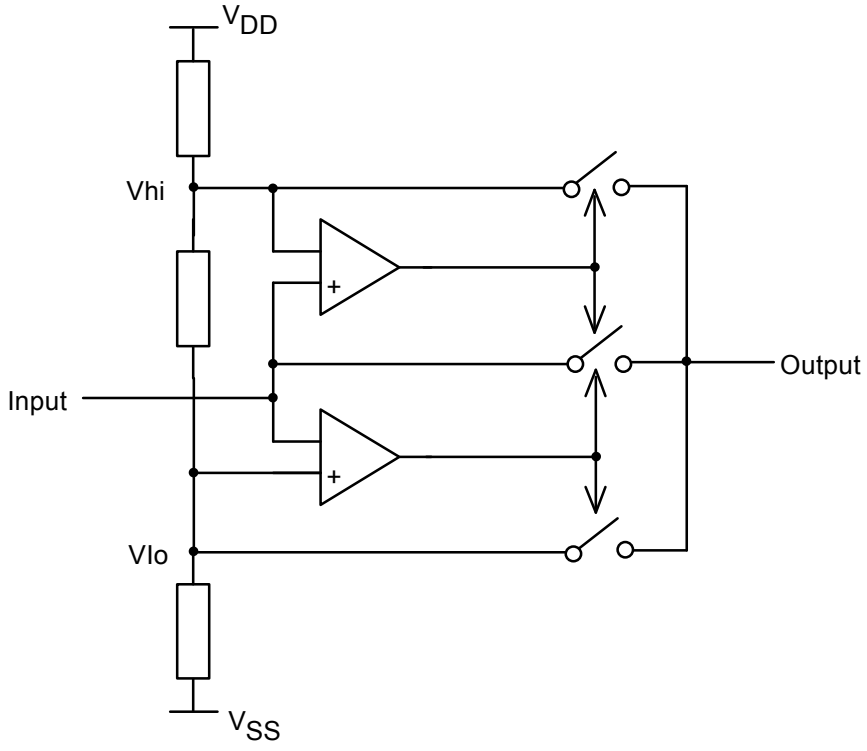
Description

This minor ACSC function is a limiter consisting of two comparators and three switches that clamp the output to the high and low limiting voltages. This type of circuit operates with signals from DC to audio frequencies. The speed of the comparator will determine the upper frequency response of the limiter. The reference voltages can either be generated as a ratio of the supply voltages, as shown, or derived from a known reference, for example a bandgap.

Features

- Operates from DC to audio frequencies
- Limiting levels set by resistor ratio

Functional Block Diagram



SOFT LIMITER

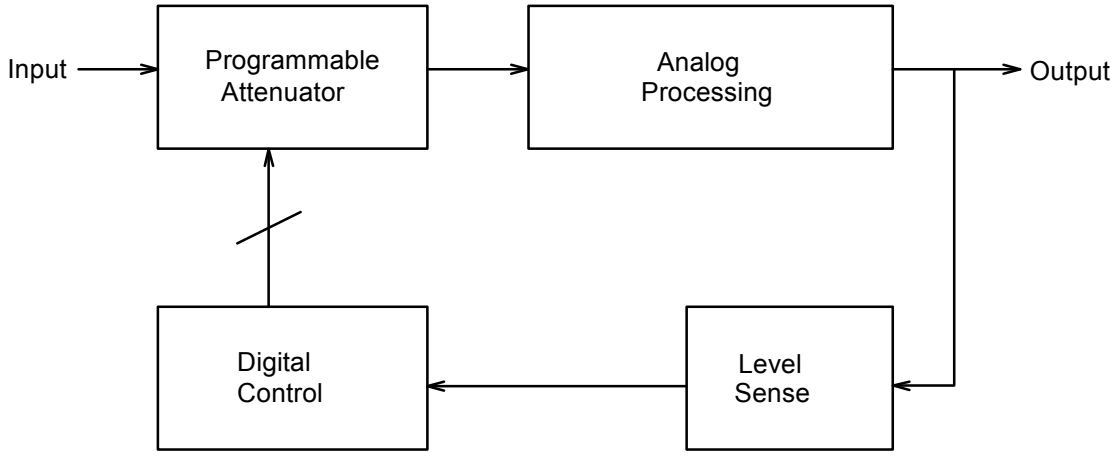
Description

This minor ACSC function is a soft limiter consisting of a gain stage, level sense and digital controller in a closed loop. The signal amplitude is controlled using a digitally programmable attenuation stage driven from an up/down counter. The attack and decay rates are set in the up/down count speed. The level sensing occurs after any system signal processing (for example filtering) and causes the digital control to count up when the preset limit is exceeded.

Features

- Attack/decay time set in digital controller
- Level sensing requires only a simple comparator
- Preset limit for the sense can easily be made ratiometric with supply voltage

Functional Block Diagram



CLOCK SQUARER

Description

This minor ACSC function is a clock squarer consisting of a fast comparator nested within an integrator loop. The loop provides a slow time-averaged dc threshold for the comparator.

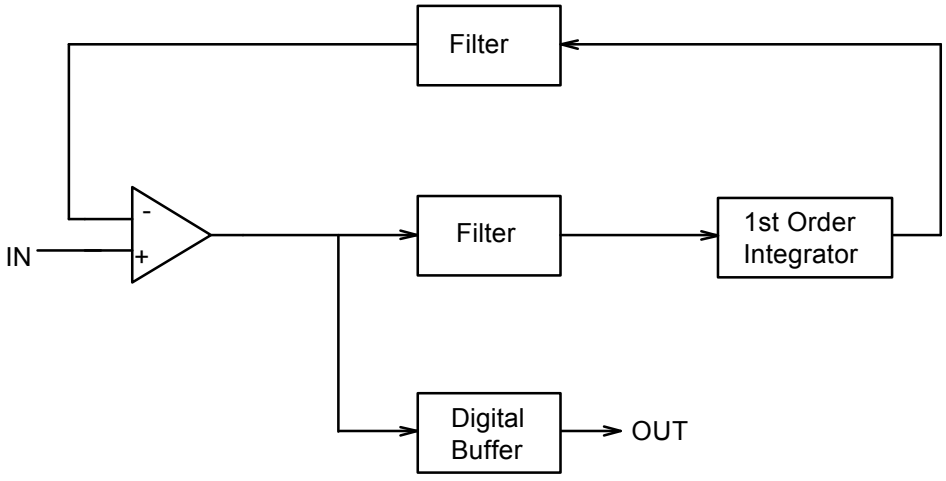
A 1% accurate 50-50 duty cycle square wave, at up to 20MHz, is produced for signal levels as low as 400mVpp within a 2V dc range.

Time constant of integrator loop ≈ 10µs.
Quiescent supply current approximately 400µA.

Features

- Provides stable clock with 50-50 duty cycle from a low-level distorted sine/square input
- Internal dc tracking of input signal
- Operation up to 20MHz

Functional Block Diagram



FULL WAVE RECTIFIER

Description

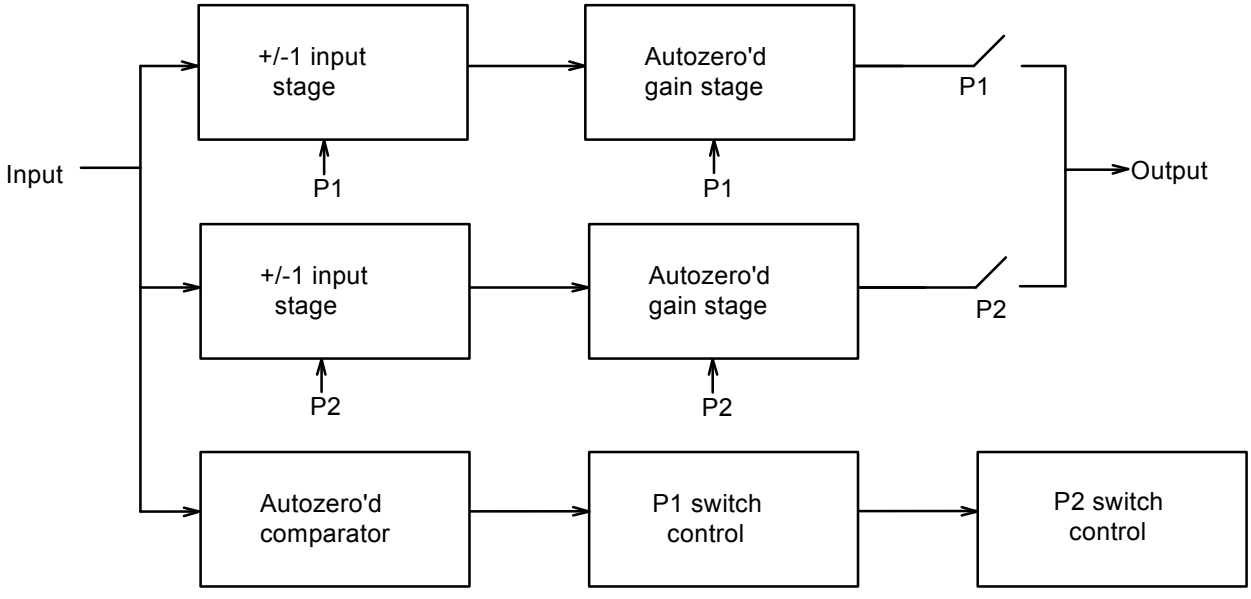
This minor ACSC function is a full wave rectifier, built using two interleaved rectifiers to generate a continuous output. Each rectifier consists of a +/-1 gain stage followed by an autozero'd switched capacitor gain stage. This cancels any amplifier input offset and gives an accurate gain (due to the matching of the capacitor ratio).

The polarity of the input is sensed using an autozero'd comparator that drives the P1 and P2 switch control circuits.

Features

- Low input offset circuit
- Continuous output
- Accurate gain due to SC structure

Functional Block Diagram



MANCHESTER ENCODER

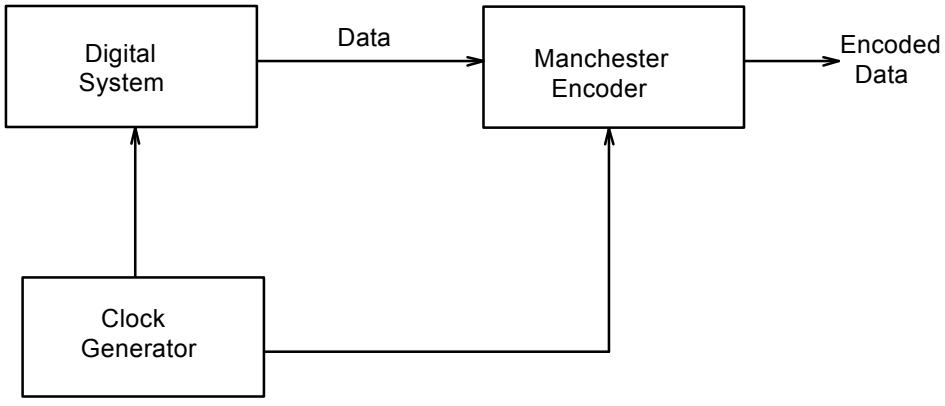
Description

This minor ACSC function provides Manchester coding or digital biphase coding which is used in many applications, for example in Ethernet local area networks. The attraction of this type of coding of the data is that it contains a strong timing component and zero DC spectral content. In digital biphase coding, one cycle of a square wave with a particular phase is used to indicate a 0. Since there is a transition at the centre of every symbol interval a strong timing signal is available for synchronisation.

Features

- Data contains timing information
- Simple implementation

Functional Block Diagram



BATTERY VOLTAGE DETECTOR

Description

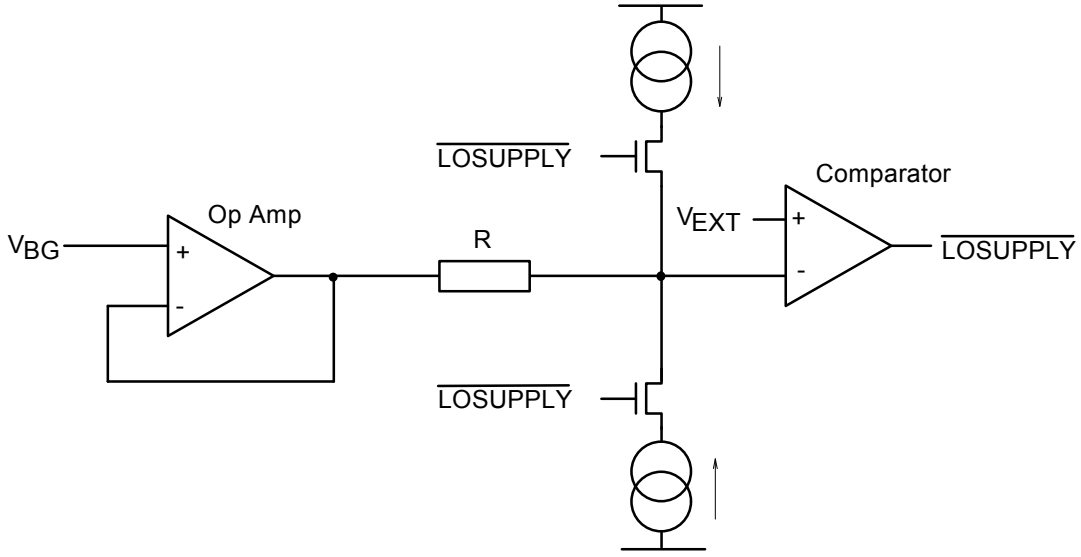
This minor ACSC function is a battery voltage monitor where a buffered bandgap reference voltage is compared to an external voltage, and output LOSUPPLY goes low when $V_{EXT} < V_{TRIP}$. The use of the bandgap reference voltage allows an accurate and temperature stable threshold to be defined.

The positive trip level, as V_{EXT} falls towards V_{BG}, is V_{BG} - IR. When $V_{EXT} < V_{BG}$ - IR, LOSUPPLY goes low, moving V_{TRIP} to V_{BG} + IR. Appropriate choice of I and R allows any noise on V_{EXT} to be rejected, and not cause false triggering of LOSUPPLY.

Features

- Comparator and bandgap reference voltage allows accurate voltage detection
- Incorporates hysteresis to prevent false triggering and output glitches
- Use of external potentiometer allows voltages outside of the supply range of the device to be monitored
- Useful in low battery voltage detection circuits

Functional Block Diagram



VOLTAGE REGULATOR

Description

This minor ACSC function is a 5V voltage regulator and requires just 1 resistor, 1 diode, 1 npn transistor and 1 capacitor to function. It is capable of providing up to 12mA at 5V. The output is accurate to 10% over the temperature range 0-70ºC and for input voltages between 6V and 16V.

Features

- 6-16V input voltage range
- 5V ±10% output voltage
- 12mA current capability
- Uses just 4 external components

Functional Block Diagram